Amendments to the Specification

Please replace paragraph [0035] with the following amended paragraph:

[0035] The dielectric layer 20 has an oxide-nitride-oxide (ONO) structure in which a first oxide film 14, a nitride film 16 and a second oxide film 18 are disposed one atop the other on the substrate 10. The first oxide film 14 serves as a tunneling oxide film and the second oxide film ~~16~~ 18 functions as a blocking oxide film.

Please replace paragraph [0090] with the following amended paragraph:

[0090] One ~~On a~~ feature of the invention is to provide a method of manufacturing an efficiently programmable non-volatile semiconductor device.

Please replace paragraph [0120] with the following amended paragraph:

[0120] In accordance with another aspect of the present invention, after a dielectric layer pattern having an ONO composition is formed on the substrate, the substrate by exposed the dielectric layer pattern is oxidized.

Please replace paragraph [0175] with the following amended paragraph:

[0175] Subsequently, the etching mask is removed, and a second photoresist pattern that exposes a portion of the dielectric layer pattern is formed on the semiconductor substrate. The exposed portion of the dielectric layer pattern ~~patterns~~ is etched a certain amount using the polysilicon layer pattern as an etching mask (step S160). That is, the exposed dielectric layer pattern is etched using a self-alignment etching process. At this time, the second oxide film pattern and the

nitride film pattern of the exposed dielectric layer pattern are removed. However, a remaining portion of the exposed dielectric layer pattern, such as the first oxide film pattern, is left to serve as a buffer layer that protects the semiconductor substrate during an ion implantation process for forming source/drain regions. In addition, the remaining portion of the exposed dielectric layer pattern can prevent damage to the substrate, including to the drain region, when an etch back process is carried out to form a spacer on a sidewall of the polysilicon layer pattern.